

American International University- Bangladesh

Department of Faculty of Engineering

EEE 3102: Digital Logic & Circuits Laboratory

**Title:** Construction Logic Gates using various MOS transistors

**Part I: Construction of MOSFET Logic Gates**

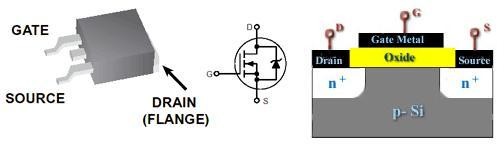
# Introduction:

### MOSFET:

Pronounced MAWS-feht. Acronym for metal-oxide semiconductor field-effect transistor. These are used in many scenarios where you want to convert voltages. On your motherboard for example to generate CPU Voltage, Memory Voltage, AGP Voltage etc. Mosfets are usually used in pairs. If you see six mosfets around your CPU socket you have three-phase power.

### Technical Info

MOSFETs come in four different types. They may be enhancement or depletion mode, and they may be n-channel or p-channel. For this application we are only interested in n-channel enhancement mode MOSFETs, and these will be the only ones talked about from now on. There are also logic-level MOSFETs and normal MOSFETs. The only difference between these is the voltage level required on the gate.



Unlike bipolar transistors that are basically current-driven devices, MOSFETs are voltage-controlled power devices. If no positive voltage is applied between gate and source the MOSFET is always non- conducting. If we apply a positive voltage UGS to the gate we'll set up an electrostatic field between it and the rest of the transistor. The positive gate voltage will push away the 'holes' inside the p-type substrate and attracts the moveable electrons in the n-type regions under the source and drain electrodes. This produces a layer just under the gate's insulator through which electrons can get into and move along from source to drain. The positive gate voltage therefore 'creates' a channel in the top layer of material between oxide and p-Si. Increasing the value of the positive gate voltage pushes the p-type holes further away and enlarges the thickness of the created channel. As a result we find that the size of the channel we've made increases with the size of the gate voltage and enhances or increases the amount of current which can go from source to drain- this is why this kind of transistor is called an enhancement mode device. Hence the operation of a p-channel MOSFET is just the opposite of an n-channel MOSFET.

### MOSFET testing

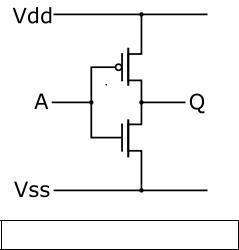
Get a multimeter with a diode test range. Connect the meter negative to the MOSFET's source. Hold the MOSFET by the case or the tab if you wish, it doesn't matter if you touch the metal body but be careful not to touch the leads until you need to. Do NOT allow a MOSFET to come in contact with your clothes,

plastic or plastic products, etc. because of the high static voltages it can generate. First touch the meter positive on to the gate. Now move the positive meter probe to the drain. You should get a low reading. The MOSFET's gate capacitance has been charged up by the meter and the device is turned on. With the meter positive still connected to the drain, touch a finger between source and gate (and drain if you wish, it doesn't matter). The gate will be discharged through your finger and the meter reading should go high, indicating a non-conducting device.

### CMOS:

**Complementary metal–oxide–semiconductor** (**CMOS**) is a technology for constructing [integrated](http://en.wikipedia.org/wiki/Integrated_circuit) [circuits.](http://en.wikipedia.org/wiki/Integrated_circuit) CMOS technology is used in [microprocessors,](http://en.wikipedia.org/wiki/Microprocessor) [microcontrollers,](http://en.wikipedia.org/wiki/Microprocessor) [static RAM,](http://en.wikipedia.org/wiki/Static_Random_Access_Memory) and other [digital](http://en.wikipedia.org/wiki/Digital_logic) [logic](http://en.wikipedia.org/wiki/Digital_logic) circuits. CMOS technology is also used for several analog circuits such as [image sensors (CMOS](http://en.wikipedia.org/wiki/Image_sensor) [sensor),](http://en.wikipedia.org/wiki/CMOS_sensor) [data converters,](http://en.wikipedia.org/wiki/CMOS_sensor) and highly integrated [transceivers](http://en.wikipedia.org/wiki/Transceiver) for many types of communication. [Frank](http://en.wikipedia.org/wiki/Frank_Wanlass) [Wanlass](http://en.wikipedia.org/wiki/Frank_Wanlass) patented CMOS in 1963 [(US patent 3,356,858).](http://en.wikisource.org/wiki/United_States_patent_3356858)

CMOS is also sometimes referred to as **complementary-symmetry metal–oxide–semiconductor** (or COS-MOS). The words "complementary-symmetry" refer to the fact that the typical digital design style with CMOS uses complementary and symmetrical pairs of [p-type](http://en.wikipedia.org/wiki/P-type_semiconductor) and [n-type metal oxide semiconductor](http://en.wikipedia.org/wiki/N-type_semiconductor) [field effect transistors](http://en.wikipedia.org/wiki/Metal_oxide_semiconductor_field_effect_transistor) (MOSFETs) for logic functions.



CMOS inverter ([NOT logic gate](http://en.wikipedia.org/wiki/Inverter_%28logic_gate%29))

Two important characteristics of CMOS devices are high [noise immunity](http://en.wikipedia.org/wiki/Electronic_noise) and low static [power](http://en.wikipedia.org/wiki/Power_consumption) [consumption.](http://en.wikipedia.org/wiki/Power_consumption) Since one [transistor](http://en.wikipedia.org/wiki/Transistor) of the pair is always off, the series combination draws significant power only momentarily during switching between on and off states. Consequently, CMOS devices do not produce as much [waste heat](http://en.wikipedia.org/wiki/Waste_heat) as other forms of logic, for example [transistor–transistor logic](http://en.wikipedia.org/wiki/Transistor%E2%80%93transistor_logic) (TTL) or [NMOS logic,](http://en.wikipedia.org/wiki/NMOS_logic) which normally have some standing current even when not changing state. CMOS also allows a high density of logic functions on a chip. It was primarily for this reason that CMOS became the most used technology to be implemented in [VLSI](http://en.wikipedia.org/wiki/VLSI) chips.

Some advantages of CMOS over TTL are:

* CMOS gate inputs draw far less current than TTL inputs, because MOSFETs are voltage- controlled, not current-controlled, devices.
* CMOS gates are able to operate on a much wider range of power supply voltages than TTL: typically 3 to 15 volts versus 4.75 to 5.25 volts for TTL
* CMOS transistors are smaller in size and provide less power dissipation than NMOS transistors.

In this experiment, we will first look at some logic circuit designs using NMOS. Then we will implement the same logic circuits using CMOS and try to identify the potential design advantages of CMOS over NMOS.

# Theory and Methodology:

#### NMOS Inverter with Ohmic/ Resistive Load:

Considering an ideal scenario, when a HIGH (+5V) is applied to the input, the NMOS transistor turns ON and current flows from Vdd to ground; thus output voltage, Vo= 0V.

Similarly, if a LOW (0V) is applied to the input, the NMOS remains in its OFF state. As a result, the current from Vdd has no path to ground. The output voltage is +5V

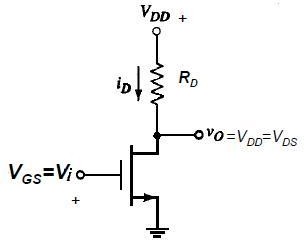


Fig.1: NMOS Inverter with Ohmic/Resistive Load

#### NMOS Inverter with NMOS Enhancement Transistor load:

One disadvantage of designing NMOS logic circuits with ohmic load is that even when the NMOS is OFF, there is static power dissipation due to the resistor. A better design is to use an enhancement-type NMOS as load. They are “*normally-off”* devices and it takes an applied voltage between gate and drain of the correct polarity to bias them *on*. Thus static power consumption is avoided

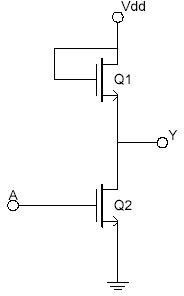
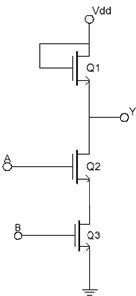


Fig.2 NMOS Inverter with NMOS Load

#### NMOS NAND Gate:



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Fig.3 NMOS NAND Gate

#### NMOS NOR Gate:

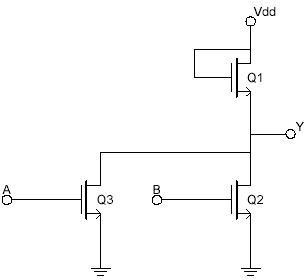


Fig.4 NMOS NOR Gate

#### CMOS Logic:

CMOS transistors are smaller in size and provide less power dissipation than NMOS transistors. Thus they became the obvious choice of replacing NMOS transistors at the integrating circuit level design in all applications.

CMOS consists of one p-channel MOSFET or PMOS and one NMOS. The two MOSFETs are designed to have matching characteristics. Thus, they are complementary to each other. When OFF, their resistance is effectively infinite; when ON, their channel resistance is quite low (around 200 Ω). Since the gate is essentially an open circuit it draws no current and the output voltage will be equal to either ground or to the power supply voltage, depending on which transistor is conducting.

#### CMOS Inverter:

When the input is grounded (logic 0), the N-channel MOSFET is unbiased, and therefore has no channel enhanced within itself. It is an open circuit, and therefore leaves the output line disconnected from ground. At the same time, the P-channel MOSFET is forward biased, so it has a channel enhanced within itself. This channel has a resistance of about 200 Ω, connecting the output line to the +V supply. This pulls the output up to +V (logic 1).

When input A is at +V (logic 1), the P-channel MOSFET is off and the N-channel MOSFET is on, thus pulling the output down to ground (logic 0). Thus, this circuit correctly performs logic inversion, and at the same time provides active pull-up and pull-down, according to the output state.

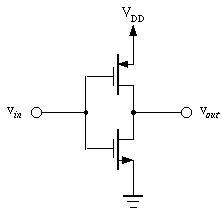


Fig.5 CMOS Inverter

#### CMOS NAND Gate:

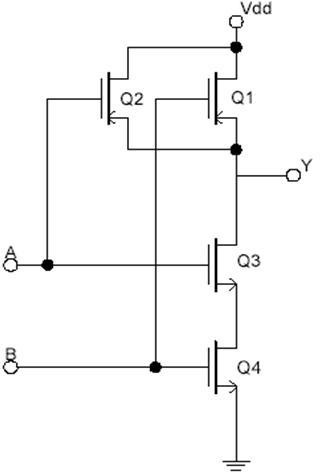


Fig.6 CMOS NAND Gate

#### CMOS NOR Gate:

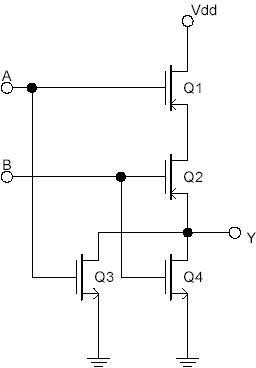
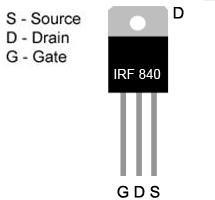


Fig.7 CMOS NOR Gate

**MOSFET pin configuration:**



**Pre-Lab Homework:**

1. Develop truth tables for a 2-input NAND and a 2-input NOR gate.

truth tables for a 2-input NAND truth tables for a 2-input NAND

|  |  |  |
| --- | --- | --- |
| A | B | Y |
| 0 | 0 | 1 |
| 0 | 1 | 1 |
| 1 | 0 | 1 |
| 1 | 1 | 0 |

|  |  |  |
| --- | --- | --- |
| A | B | Y |
| 0 | 0 | 1 |
| 0 | 1 | 0 |
| 1 | 0 | 0 |
| 1 | 1 | 0 |

1. Explain with graphs the I-V characteristics of different types of MOSFET.

**Here's a brief explanation of the I-V characteristics of different types of MOSFETs with simplified graphs:**

1. NMOS (n-channel Enhancement-mode MOSFET)

Cut-off Region (Vgs < Vt):No significant current flows when the gate-source voltage (Vgs) is below the threshold voltage (Vt)

Triode (Ohmic) Region (Vgs > Vt and Vds < Vgs - Vt) Current increases linearly with drain-source voltage (Vds) while the NMOS is in the triode region.

Saturation Region (Vgs > Vt and Vds ≥ Vgs - Vt):The NMOS is fully on, and the current saturates.

2.PMOS (p-channel Enhancement-mode MOSFET):

Cut-off Region (Vgs > Vt): Similar to NMOS, no significant current flows when Vgs is below Vt.

Triode (Ohmic) Region (Vgs < Vt and Vds < Vgs - Vt) Current increases linearly with Vds while the PMOS is in the triode region.

A diagram of a voltage current

Description automatically generated Saturation Region (Vgs < Vt and Vds ≥ Vgs - Vt):The PMOS is fully on, and the current saturates.

3. Depletion-mode MOSFET (Enhancement-type):

Depletion-type MOSFETs:Normally conductive even without an applied voltage. The gate-source voltage modulates the channel conductance.

In summary, the I-V characteristics of MOSFETs show distinct regions of operation based on the applied gate-source voltage and drain-source voltage. Understanding these characteristics is crucial for designing and analyzing electronic circuits, especially in digital and analog applications.

1. Distinguish the similarities and differences between a MOSFET and FET.

#### the similarities between MOSFET and FET:

#### **Both are three-terminal devices:** They have a source, drain, and gate electrode.

#### **Both control current flow:** The gate voltage controls the flow of current between the source and drain.

#### **Both are used in amplifiers and switches:** They can amplify signals and act as electronic switches.

#### **Both are voltage-controlled devices:** The gate voltage controls the output current.

#### the differences between MOSFET and FET:

|  |  |  |
| --- | --- | --- |
| Feature | MOSFET | FET |
| Gate structure | Insulated gate (SiO2) | No insulating layer |
| Current control mechanism | Electric field effect | Depletion of charge carriers |
| Operation mode | Enhancement-mode (default off) and depletion-mode (default on) | Depletion-mode only |
| Gate current | Very low | Relatively high |
| Input impedance | Very high | High |
| Output impedance | Low | Moderate |
| Noise figure | Low | Relatively high |
| Manufacturing cost | High | Low |
| Applications | High-performance analog and digital circuits | Low-noise amplifiers and voltage-controlled resistors |

Students must install PSpice/LTSpice/ Psim software and MUST present the simulation results using transistors to the instructor before the start of the experiment.

### Apparatus:

1. 10KΩ resistor (brown-black-orange).
2. 1N914 diodes or equivalent.
3. Connecting wires. (4)Trainer Board **Precautions:**

Have your instructor check all your connections after you are done setting up the circuit and make sure

that you apply only enough voltage (within VDD) to turn on the transistors and/or chip, otherwise it may get damaged.

# Experimental Procedure:

* 1. Set up the circuit for NMOS inverter as shown in Fig.1.

A screenshot of a computer

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* 1. Repeat steps 1 and 2 for each circuit set-up from Fig.2 to Fig. 7.

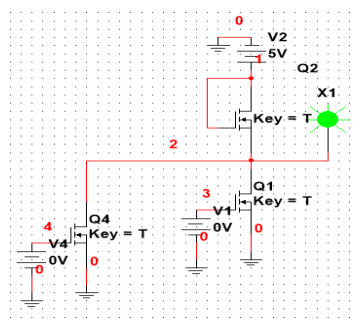
A diagram of a circuit

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A diagram of a circuit

Description automatically generatedNMOS Inverter with NMOS Enhancement Transistor load

NMOS NAND Gate



NMOS NOR Gate

A diagram of a circuit

Description automatically generated

CMOS Inverter

A diagram of a circuit

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CMOS NAND Gate:

# CMOS NOR Gate A diagram of a circuit Description automatically generated

# Results and Discussion:

In this experiment, we have used NI Multisim version -14.2 software for the Simulations. We faced some problems while finding the components in the software, that’s why it took a much extra time. The overall outcome was excellent for finding the answer using the application, and implementing the circuit was quite difficult for beginners. At first, we had to learn about Construction of MOSFET Logic Gates(mosfet,cmosfet,nmosfet). After that, we can get ready to work with Multisim Software. Then, we successfully assembled all of the components on the Multisim bread board without any faults.

# Report:

1. Implement logic function Vout = A+ BC+ DEF using: (a) NMOS (b) CMOS

Vout = 𝑨 + using CMOS:

A computer screen shot of a diagram

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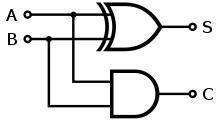
# Part II: Designing a Half Adder using CMOS

**Introduction:**

**ADDER:**

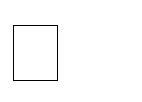
In electronics, an **adder** or **summer** is a [digital circuit](http://en.wikipedia.org/wiki/Digital_circuit) that performs [addition](http://en.wikipedia.org/wiki/Addition) of numbers. In many [computers](http://en.wikipedia.org/wiki/Computer) and other kinds of processors, adders are used not only in the [arithmetic logic unit](http://en.wikipedia.org/wiki/Arithmetic_logic_unit)(s), but also in other parts of the processor, where they are used to calculate addresses, table indices, and similar operations.

Although adders can be constructed for many numerical representations, such as [binary-coded decimal](http://en.wikipedia.org/wiki/Binary-coded_decimal) or [excess-3,](http://en.wikipedia.org/wiki/Excess-3) the most common adders operate on [binary](http://en.wikipedia.org/wiki/Binary_numeral_system) numbers. In cases where [two's complement](http://en.wikipedia.org/wiki/Two%27s_complement) or [ones' complement](http://en.wikipedia.org/wiki/Ones%27_complement) is being used to represent negative numbers, it is trivial to modify an adder into an [adder– subtractor.](http://en.wikipedia.org/wiki/Adder%E2%80%93subtractor) Other [signed number representations](http://en.wikipedia.org/wiki/Signed_number_representations) require a more complex adder.



## Fig-1 Half adder logic diagram

The **half adder** adds two single binary digits *A* and *B*. It has two outputs, sum (*S*) and carry (*C*). The carry signal represents an overflow into the next digit of a multi-digit addition. The value of the sum is 2*C*

*S*. The simplest half-adder design, pictured above, incorporates an [XOR gate](http://en.wikipedia.org/wiki/XOR_gate) for S and an [AND gate](http://en.wikipedia.org/wiki/AND_gate) for C. With the addition of an OR gate to combine their carry outputs, two half adders can be combined to make a full adder.

The half-adder adds two input bits and generate carry and sum which are the two outputs of half-adder. The input variables of a Half adder are called the Augend and addend bits. The output variables are the Sum and Carry. The

Truth table and equations for the Half adder are :



|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| **A** | **B** | **A+B** | **S** | **C** |
| 0 | 0 | 0 | 0 | 0 |
| 0 | 1 | 1 | 1 | 0 |
| 1 | 0 | 1 | 1 | 0 |
| 1 | 1 | 2 | 0 | 1 |

This experiment is to help the student in understanding the design at the transistor level.

# Theory and Methodology:

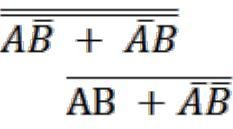
To design any logic circuit first the truth table is needed to be established using different combinations of logic ‘0’ and ‘1’ to get the desired output. After that the gate level design is found from which transistor level design is done using desired transistors. Here CMOS is used for the transistor level design of the Half Adder. The whole process is given step wise below:

# Half Adder:

## Gate Level Design:

Fig-2 Logic diagram of a Half Adder.

Equation of Sum = A (XOR) B



=  +

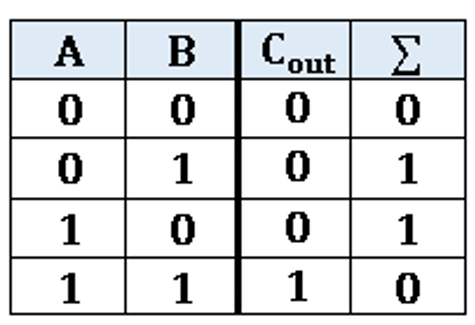
This equation can be rewritten as =

=

Equation of Carry= AB

# Pre-Lab Homework:

* 1. Develop the Truth table for a half adder.

Half-Adder Truth Table

|  |  |
| --- | --- |
| **Simulation** | **Hardware** |
| **A=0, B=0 , Sum=0** | **A=0, B=0 , Sum=0** |
| **A=1, B=0 , Sum=1** | **A=1, B=0 , Sum=1** |

|  |  |
| --- | --- |
| **Simulation** | **Hardware** |
| **A=0, B=1, Sum=1** | **A=0, B=1, Sum=1** |
| **A=1, B=1 , Sum=0** | **A=1, B=1 , Sum=0** |
| **A=0, B=0 , Carry=0** A screenshot of a computer  Description automatically generated | **A=0, B=0 , Carry =0** A circuit board with wires and switches  Description automatically generated |
| **A=1, B=0 , Carry =0 A screenshot of a computer  Description automatically generated** | **A=1, B=0 , Carry =**A circuit board with wires and switches  Description automatically generated**0** |

|  |  |
| --- | --- |
| **Simulation** | **Hardware** |
| **A=0, B=1, Carry=**A screenshot of a computer  Description automatically generated**0** | **A=0, B=1, Carry=****0** |
| **A=1, B=1 , Carry =A screenshot of a computer  Description automatically generated1** | **A=1, B=1 , Carry =**A close-up of a circuit board  Description automatically generated**1** |

* 1. Develop the truth table for a full adder along with circuit diagram and equations. Explain the equations.

A table with numbers and symbols

Description automatically generatedTruth Table:

# Apparatus:

1. PMOS,
2. NMOS,
3. IC 7404(Inverter).
4. Connecting wires.
5. Trainer Board

# Precautions:

Have your instructor check all your connections after you are done setting up the circuit and make sure that you apply only enough voltage (within VDD) to turn on the transistors and/or chip, otherwise it may get damaged.

# Experimental Procedure:

Construct the Half adder circuit using CMOS on your breadboard based on provided expression and truth table. At first draw the schematic circuit diagram for the SUM and CARRY then show to the Instructor. After that record the values in the table below.

|  |  |  |  |
| --- | --- | --- | --- |
| Input A | Input B | Carry Out | Sum |
| 0 V | 0 V | 0 | 0 |
| 0 V | 5 V | 0 | 1 |
| 5 V | 0 V | 0 | 1 |
| 5 V | 5 V | 0 | 0 |

# Report:

## A screenshot of a computer Description automatically generatedDocument the data acquired from the hardware, from simulation as well as the expected values for the CarryOut and Sum of the Half Adder.

Half Adder using CMOS Simulation:

* + 1. A diagram of a circuit

       Description automatically generatedDraw the circuit diagram of a Full Adder using CMOS.

Full Adder using CMOS

# Results and Discussion:

We will summarize the experiment and discuss it. Interpret the data/findings and determine the extent to which the experiment was successful in complying with the goal that was initially set. In lab Some experimental value mismatch for not proper equipment so sometime mismatch experimental and simulation value.

**Reference(s):**

1. Thomas L. Floyd, *Digital Fundamentals*, 9th Edition, 2006, Prentice Hall.
2. Link: <http://www.techpowerup.com/articles/overclocking/voltmods/21>